Combined Finned Microgap with Dedicated Extreme-Microgap Hotspot Flow for High Performance Thermal Management

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ABSTRACT

There are a number of emerging electronic applications that are thermally limited and may exhibit high overall power dissipation ("background") combined with local very high power fluxes ("hotspot"). We have batch fabricated a microfluidic heat sink specifically designed to address both levels of heat removal. A microgap for hotspot cooling and micropin-fins are sequentially deep etched in a silicon substrate. The combined microfluidic heat sink is sealed by bonding another layer of silicon to the substrate. The coolant is injected into the combined heat sink from two distinct ports to dissipate the generated heat by micro-heaters. These micro-heaters emulate hotspot and background heat generation by active circuits as well as enable chip junction temperature measurement. Mechanical modeling is conducted to verify the reliability of the design and assess limits on the operating pressure of the fabricated system.

KEY WORDS: Hotspot cooling, microfluidic cooling, boiling heat transfer, microgap, liquid cooling

I. INTRODUCTION

In this work, we propose to address background and hotspot cooling challenges simultaneously by exploiting two-phase (boiling) microfluidic cooling technology [1]. A hybrid microfluidic heat sink embedded in the silicon is implemented and features a microgap region for hotspot cooling integrated with a hydro-foil micro-pin fins for background cooling. Specifically, a high pressure (~ 2.0 MPa) refrigerant (R134a) is provided though separate fluidic vias to two separately purposed microgaps, sized differently for background and hotspot requirements. In both RF and digital applications, thermal maps are non-uniform due to the non-uniform power dissipation, which necessitates the use of a targeted cooling scheme. In this design, a larger microgap (1 cm x 1 cm x 200 µm height) with integrated micropin-fins has been formed using a hydrodynamic design to handle greater overall mass flow rates. Moreover, the designed fins in this large microgap enhance the heat transfer coefficient. This can accommodate high background power loads without excessive pressure drop. In parallel, smaller microgaps with shorter height (200 µm x 200 µm x 10 µm height) support very high mass flux for managing the high heat flux. Fluid is directly injected within a narrow gap near the hotspot location to achieve high heat flux removal as the refrigerant rapidly boils. The hotspot flow effluent exits the hotspot zone and mixes with the background flow with little impact on the background coolant enthalpy due to the relatively small total power dissipated in the hotspot. Because of the high pressure conditions, which are necessary for effective boiling using refrigerants [2], the device reliability is a concern. To successfully mitigate failure due to pressure, structural models are created to determine the placement of structural supports within the combined heat sink architecture. A study is conducted with this model to evaluate the effects of wafer thickness on the stress levels. This modeling results in design and processing guidelines, which are utilized in the fabrication methodology. The combined flow strategy requires innovative microfabrication approaches and relies on flow boiling heat transfer in geometries and under refrigerant flow conditions not previously characterized.

II. FABRICATION

The fabrication process involves nine overall steps including seven photolithography steps. The simplified fabrication process flow is illustrated in Fig. 1.

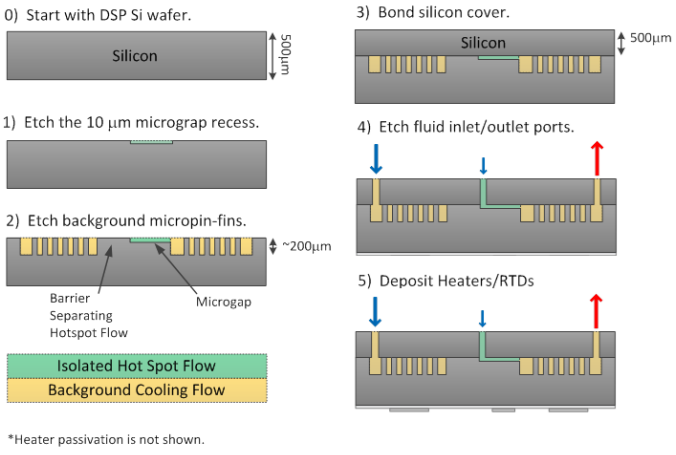

Fig. 1. Fabrication process flow illustrating hotspot microgap etching, background micropin-fins etching, silicon-silicon bonding, and metallization.

A double-side polished (DSP) 500 µm thick silicon wafer is used as the substrate. Standard Acetone-Methanol-Isopropanol (AMI) pre-cleaning steps under class 100 cleanroom environment is implemented on the bare silicon substrate. Next, the substrate is cleaned in 120ºC piranha solution for 10 min

followed by deionized water (DIW) rinsing for 2 min (i.e. step 0 in Fig. 1). Next, the hotspot microgaps are patterned through a bright-field fused-silica mask and UV lithography at 365 nm wavelength. The sample is exposed to a gentle oxygen plasma for 45 sec (i.e. descum) in a reactive-ion-etching (RIE) tool to ensure the developed features are not masked with any possible thin photoresist residue [3]. Next, the hotspot microgap is etched to a depth of 10 µm in the silicon substrate through an optimized Bosch process using an STS-ICP tool (i.e. step 1 in Fig. 1). Since the microgap is shallow (i.e. 10 µm), conventional Bosch etching recipes that are designed for deep silicon etching introduce surface roughness, as shown in Fig. 2. Therefore, the passivation time, etching time, and oxygen gas flow rate are optimized to achieve smooth shallow silicon etching [4].

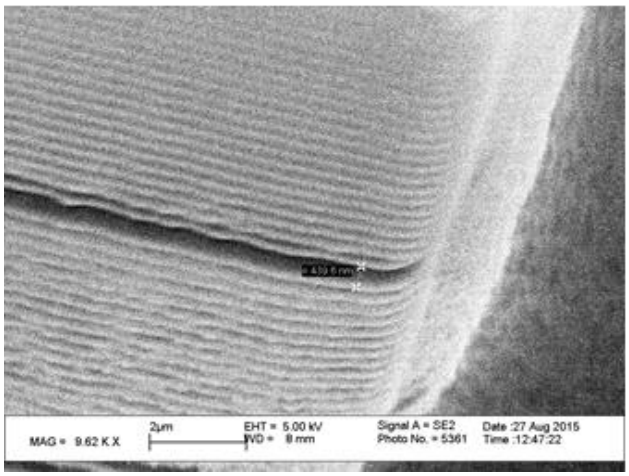

Fig. 2 Scanning electron microscopy (SEM) image of sidewall roughness resulting from a typical Bosch silicon etching process.

To prepare the silicon substrate for patterning the background micropin-fins, the initial photoresist layer is stripped off using oxygen-plasma cleaning. This procedure ensures that no photoresist residue is left on the substrate to distort subsequent fabrication steps. Fig. 3 shows the substrate with 10 µm etched features after the cleaning steps.

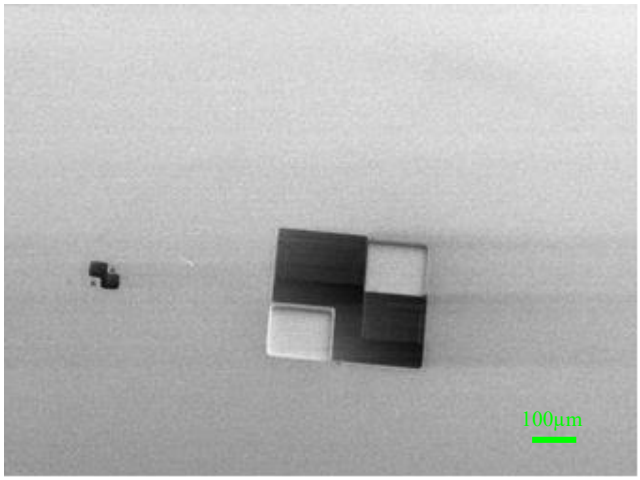

Fig. 3. Silicon substrate with multi-height etched features after AMI, piranha, and oxygen-plasma cleaning steps. The shallow feature is 10 µm deep while the second feature is 200 µm deep.

The next step of fabrication is etching the background microgaps. The background hydro-foil pin-fins are patterned and aligned with hotspot microgaps using Karl Suss TSA MA-6 mask-aligner. Next, the hydro-foil pin-fins are etched to a depth of 200 µm in the silicon substrate through an optimized Bosch process (i.e. step 2 in Fig. 1). Fig. 4 shows 200 µm tall background hydro-foil pin-fins along with 10 µm hotspot microgap on the silicon substrate.

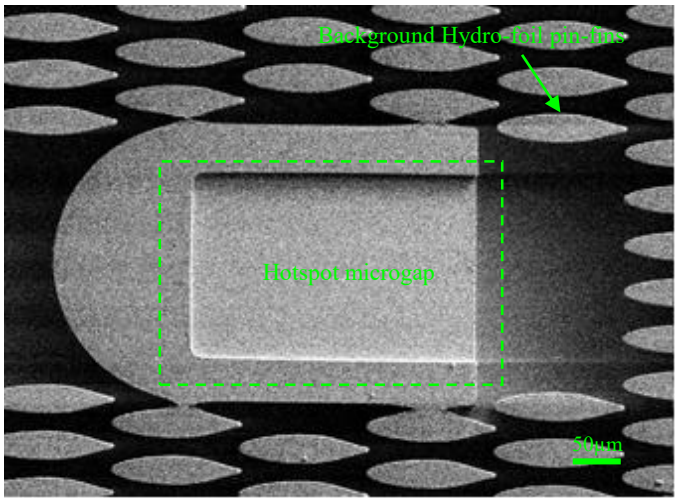

Fig. 4. SEM image of etched hotspot microgap and background micropin-fins.

The third step of fabrication is capping the etched features with a silicon wafer using activated surface silicon-silicon bonding (see Fig. 1). To achieve high strength bonding, it is important to keep the surface of both silicon substrates undamaged and clean in all fabrication steps. After aligning the substrate with the cap, pressure is applied to the sample to enhance surface bonds. Annealing cycles are employed to strengthen the bonds and prevent mechanical failure during high pressure operation. The device layout is illustrated in Fig. 5.

The fluid inlet and outlet ports are etched through the silicon cap, connecting the background ports to the reservoirs using relatively large micropin-fins. These 500 µm diameter micropin-fins are used as mechanical support structures to increase the surface area between the substrate and the cap for strengthening silicon-silicon bonding. The inlet reservoir has a dense array of micropin-fins to redistribute the coolant and regulate the fluid flow at different operating pressures. The redistribution micropin-fins are 180 µm in diameter with 350 µm x 200 µm pitch. The orientation and pitches form 20 µm vertical channels and 170 µm horizontal channels in between the micropin-fins. These narrow channels create a pressure drop at the inlet that needs to be compensated with higher pressure of operation. Furthermore, a dedicated inlet port is etched through the silicon cap above the hotspot microgap to manage the separate supply of coolant to the hotspot. Both background and hotspot have combined return flows and share one outlet. The ports are back side aligned with hotspot microgaps using Karl Suss MA-6 mask-aligner. The background ports (1.2 mm

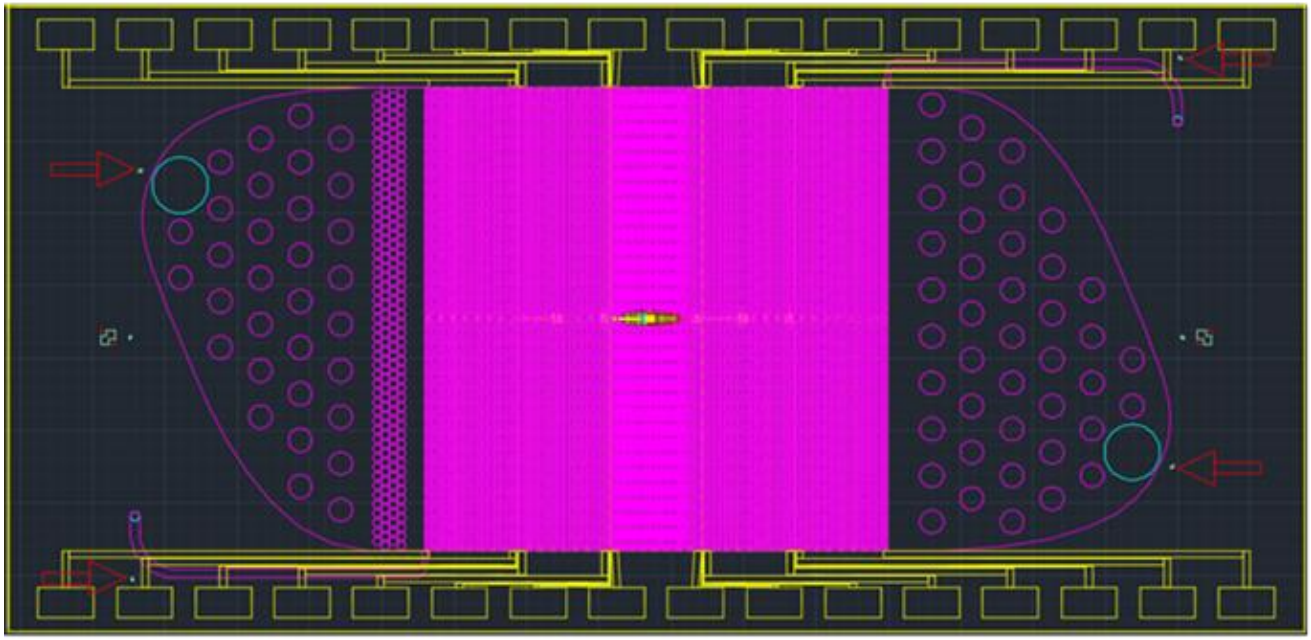

Fig. 5. Layout illustration of the complete thermal testbed; the background micro-features are pink in color. The yellow features are Pt heaters, Au wires, and Au pads. The hotspot microgap is red in color and is located at the middle of the layout. The inlet and outlet ports are represented with the blue features.

diameter) and the hotspot inlet (90 µm diameter) are simultaneously etched through the silicon cap using STS-ICP.

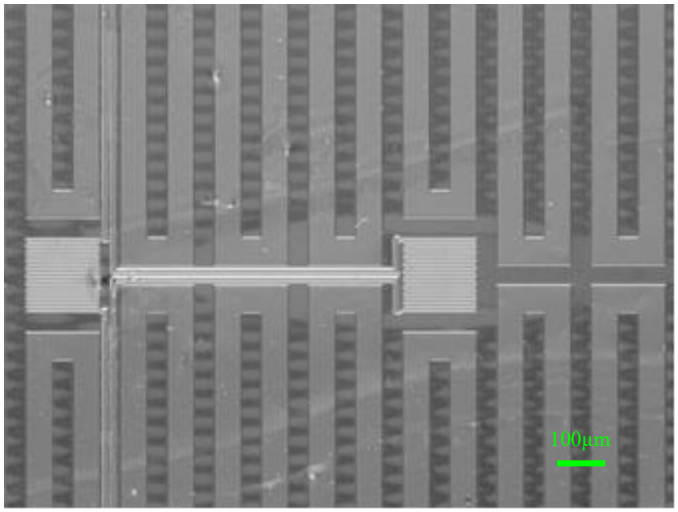

Fig. 6. Infrared (IR) image of the fully fabricated device. Pt heaters and RTDs are on the silicon cap that is bonded to the substrate. The microgaps are visible underneath the RTDs since silicon is transparent in the IR spectrum.

Since the hotspot port is 13-times smaller than background ports, the etch rate for hotspot inlet is lower and therefore the etch end-point is based on the smaller feature. After forming the ports, 2 µm silicon dioxide (SiO_2) is deposited on the top side of the sample using plasma-enhanced-chemical-vapor-deposition (PECVD). This dielectric layer electrically isolates the heaters and resistance temperature detectors (RTDs) from the silicon substrate. The RTDs and heaters are back side aligned with the inlet ports and patterned. Next, the metallization step is carried by coating the sample with 30 nm titanium (Ti) and 200 nm platinum (Pt) using a CHA metal evaporator. There are five Pt heaters for background heat generation that also serve as RTDs. The hotspot has a dedicated Pt heater/RTD, emulating high power loads. This configuration enables experiments with different background and hotspot mass fluxes. Next, gold (Au) wires and pads are aligned with the heaters and patterned (see Fig. 6). The Au pads are connected to the Pt heaters/RTDs via the Au wires. This reduces resistance and unnecessary voltage drop on the electrical connections. A 1 µm SiO_2 is deposited on the Pt elements as a passivation layer to prevent degradations, followed by Au pads reveal.

III. Fracture Modeling

Various support structures within this design are the result of thermal and reliability modeling. Through co-design, this combined heat sink architecture is intended to withstand high-pressure fluid flow. Fracture modeling is used to determine the potential for monotonic failure during pressurization. Using ANSYS® Mechanical, a structural model is developed for determining the stress distribution within the solid structure at operating pressures in excess of 2000 kPa.

The geometry is built based on the device layout (see Fig. 5). The model includes the silicon substrate into which the micropin-fins, flow ports, and supports are etched. It also includes the silicon cap, which seals the microchannel from the topside and is assumed to be perfectly bonded to the bottom silicon substrate. Heating elements and pressure ports are not included in the model as they have negligible effect on the results. The device is assumed to not be externally supported by packaging or any other constraining bodies. Fig. 7 illustrates a cross-section of the geometry.

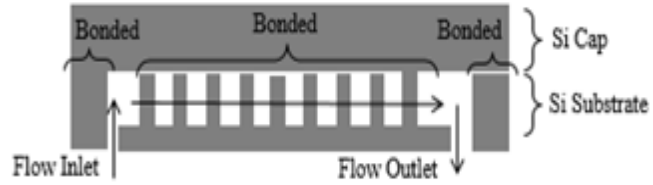

Fig. 7. Side view of the internal geometry indicating bonded regions

The material model for silicon is applied to the elements of the model. Silicon is assumed to have an anisotropic elastic modulus having stiffness matrix coefficients of 166, 64, and 80 GPa for C_{11}, C_{22}, and C_{44} respectively [5]. This system is loaded internally with a static loading pressure of 3300 kPa for the results discussed. Along with this loading condition, two nodes are pinned to prevent rigid body translation and rotation. The model is meshed using approximately $5x10^5$ elements, which takes 4 hours to solve using a 6-core processor. The stress results are shown in Figs. 8 and 9. For the given loading condition of 3300 kPa, the maximum principal stress is 189 MPa. A defect size of approximately 5 µm would be required to cause failure for this stress condition since the fracture toughness of silicon is approximately 1.0 MPa√m [6]. In prior experiments, fracture at this stress level suggests this is the approximate defect size, which is present in the structure after fabrication either through curvature of the pins or cracks in the bonding interface or possibly another unknown source. This maximum working condition of 3300 kPa allows for a significant factor of safety in excess of 1.5 assuming the actual working pressure is approximately 2000 kPa. With this modeling, the fabricated structure is shown to be reliable and capable of withstanding the operating conditions as specified during concept inception. It should be pointed that the simulation results shown here are for cylindrical pins. For hydrofoil pins, the principal stress at the tail end of the pins will be greater, and thus, the allowable operational pressure will be less.

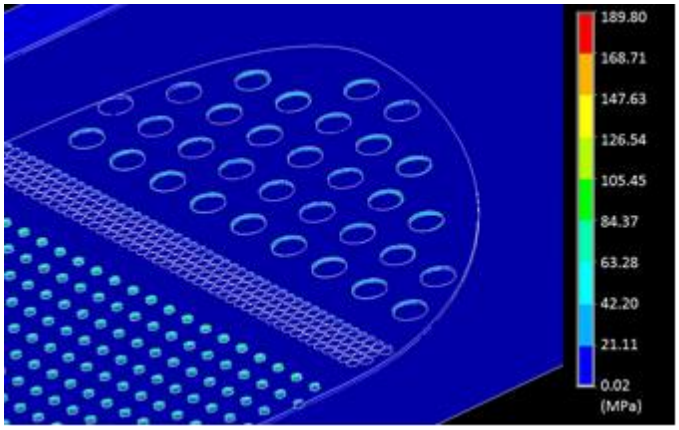

Fig. 8. Cut view of first principal stress on support pins

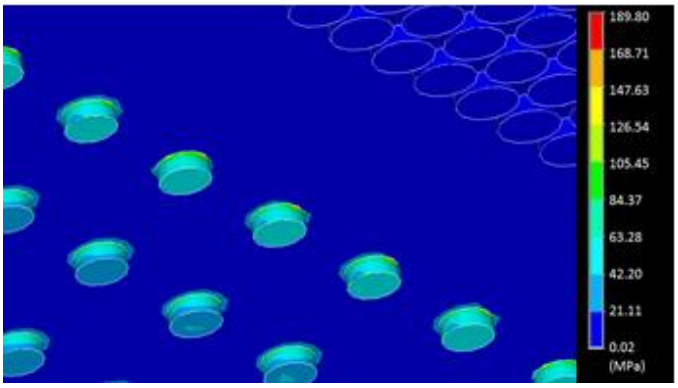

Fig. 9. Close-up view of the first principal stress on flow pins.

One critical parameter in future fabrication iterations for this design is the total thickness of the device. Reducing the wafer thicknesses of both the substrate and capping layer could have numerous benefits. Total thermal resistance of the system would be decreased for any reduction in the distance between the heaters and the microchannel. In an actual system, any stacking techniques which are implemented would also benefit from a reduced thickness in terms of electrical performance as the signal travel distance (using through-silicon vias) from level to level would be reduced. Thus both thermal and electrical performance of the device may improve for decreased wafer thicknesses. Using the established mechanical model for predicting the first principal stress during operation of these devices, a study is conducted to determine the structural effects of reducing device thickness. In this modeling study, the geometry is augmented while all boundary conditions are kept constant. Figure 10 shows the affected geometric parameter, *t*, which is varied while the height of the etched microchannel, *h*, is kept constant. The thickness of both the silicon substrate and cap are assumed to have thicknesses of 300, 400, and 500 µm for the three different cases. For the three different cases, the applied pressure within the microchannel is maintained at the same critical loading condition of 3300 kPa. The resulting maximum principal stress values are tabulated and presented in Table 1.

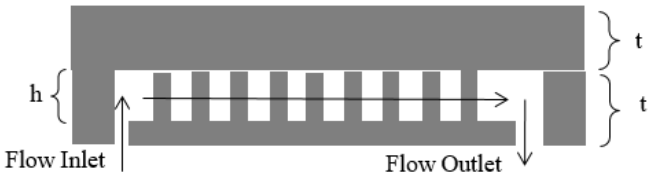

Fig. 10. Side view of internal geometry with wafer thickness, *t*, and etch depth, *h*

TABLE 1: WAFER THICKNESS STUDY RESULTS

Wafer thickness, *t*	Maximum Principal Stress
500 µm	189 MPa
400 µm	233 MPa
300 µm	285 MPa

Based on the data shown in Table 1, stress tends to increase with decreasing wafer thickness. Decreasing the cap and

substrate thicknesses from 500 μm to 300 μm results in a 51 percent increase in maximum principal stress experienced by the device. According to this trend, structural integrity and thus mechanical performance of the device will be weakened for thinner designs. Given the complex trade-offs, there should be a co-design effort to arrive at a proper balance between mechanical, electrical, and thermal aspects in future high-powered, on-chip cooling design iterations.

IV. Conclusions

A hybrid microfluidic heat sink based on two-stream cooling approach for hotspot microgap and background integration is fabricated. The manifold design is shown to have a factor of safety of 1.5 for structural stability based on the anticipated operating condition of 2000 kPa. Device thickness is expected to have a negative effect on structural integrity for the same operating conditions. Future work includes rigorous thermal and reliability testing of the testbed.

Acknowledgments

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